CS5124, CS5126

High Performance, Integrated Current Mode PWM Controllers

The CS5124/6 is a fixed frequency current mode controller designed specifically for DC−DC converters found in the telecommunications industry. The CS5124/6 integrates many commonly required current mode power supply features and allows the power supply designer to realize substantial cost and board space savings. The product matrix is as follows:

CS5124: 400 kHz w/V_{BIAS} Pin, 195 mV first current sense threshold.

CS5126: 200 kHz w/SYNC Pin, 335 mV first current sense threshold.

The CS5124/6 integrates the following features: Internal Oscillator, Slope Compensation, Sleep On/Off, Undervoltage Lock Out, Thermal Shutdown, Soft−Start Timer, Low Voltage Current Sense for Resistive Sensing, Second Current Threshold for Pulse−by−Pulse overcurrent Protection, a Direct Optocoupler Interface and Leading Edge Current Blanking.

The CS5124/6 has supply range of 7.7 V to 20 V and is available in 8 pin SOIC narrow package.

Features

- Line UVLO Monitoring
- Low Current Sense Voltage for Resistive Current Sensing
- External Synchronization to Higher or Lower Frequency Oscillator (CS5126 Only)
- Bias for Startup Circuitry (CS5124 Only)
- Thermal Shutdown
- Sleep On/Off Pin
- Soft−Start Timer
- Leading Edge Blanking
- Direct Optocoupler Interface
- 90 ns Propagation Delay
- 35 ns Driver Rise and Fall Times
- Sleep Mode
- Pb−Free Packages are Available

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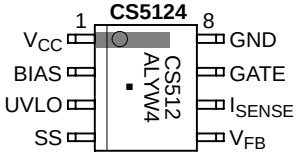
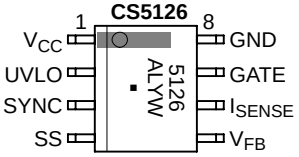
SOIC−8
D SUFFIX
CASE 751

PIN CONNECTIONS AND MARKING DIAGRAM





A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping†
CS5124XD8	SOIC−8	95 Units/Rail
CS5124XD8G	SOIC−8 (Pb−Free)	95 Units/Rail
CS5124XDR8	SOIC−8	2500 Tape & Reel
CS5124XDR8G	SOIC−8 (Pb−Free)	2500 Tape & Reel
CS5126XD8	SOIC−8	95 Units/Rail
CS5126XDR8	SOIC−8	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

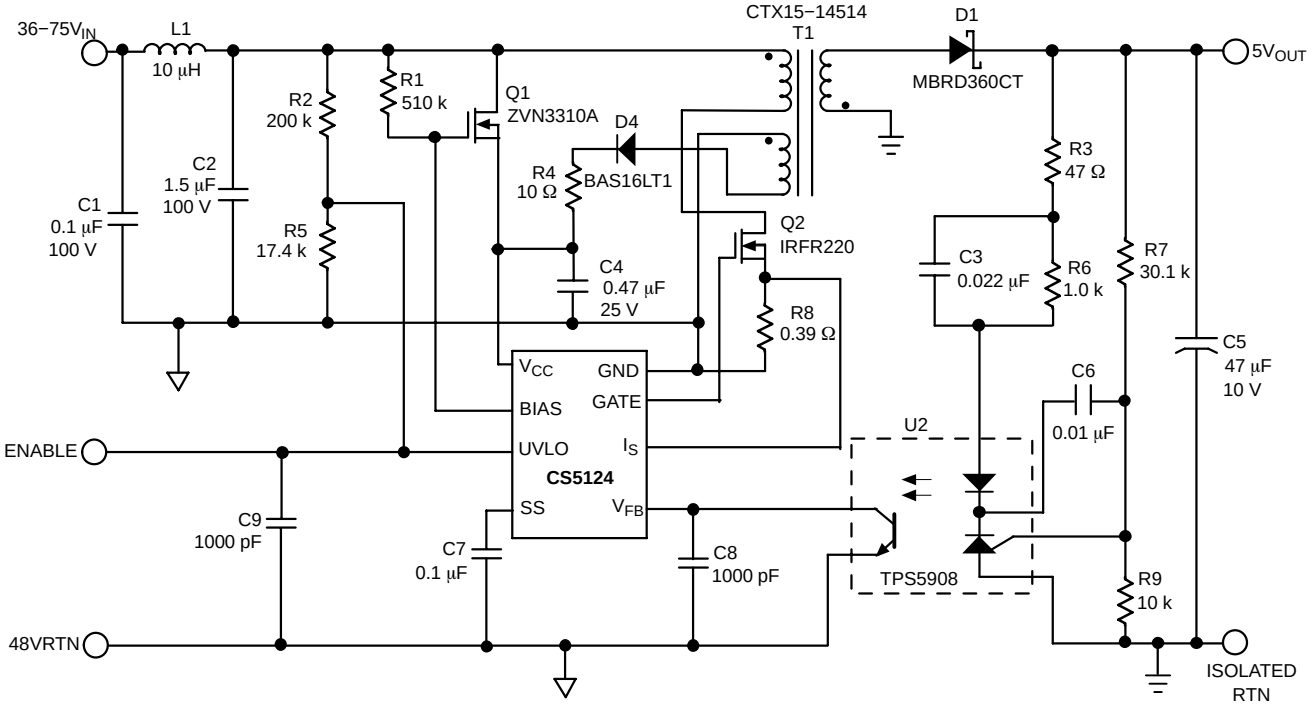


Figure 1. CS5124 Application Diagram

MAXIMUM RATINGS

Rating	Value	Unit
Operating Junction Temperature, T_J	−40 to 135	°C
Storage Temperature Range, T_S	−40 to 150	°C
ESD Susceptibility (Human Body Model)	2.0	kV
Lead Temperature Soldering: Reflow: (SMD styles only) (Note 1)	230 peak	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. 60 second maximum above 183°C.

MAXIMUM RATINGS

Pin Name	Pin Symbol	V_{MAX}	V_{MIN}	I_{SOURCE}	I_{SINK}
V_{CC} Power Input	V_{CC}	20 V	−0.3 V	1.0 mA	1.5 A Peak 200 mA DC
Clock Synchronization Input	SYNC (CS5126)	20 V	−0.3 V	1.0 mA	1.0 mA
V_{CC} Clamp Output	V_{BIAS} (CS5124)	20 V	−0.3 V	1.0 mA	1.0 mA
UVLO Shutdown Input	UVLO	6.0 V	−0.3 V	1.0 mA	1.0 mA
Soft−Start Capacitor Input	SS	6.0 V	−0.3 V	1.0 mA	2.0 mA
Voltage Feedback Input	V_{FB}	6.0 V	−0.3 V	3.0 mA	20 mA
Current Sense Input	I_{SENSE}	6.0 V	−0.3 V	1.0 mA	1.0 mA
Ground	GROUND	0 V	0 V	1.5 A peak 200 mA DC	1.0 mA
Gate Drive Output	GATE	20 V	−0.3 V	1.5 A peak 200 mA DC	1.5 A peak 200 mA DC

ELECTRICAL CHARACTERISTICS ($-40°C \le T_J \le 125°C$; $-40°C \le T_A \le 105°C$, $7.60\ V \le V_{CC} \le 20\ V$, UVLO = 3.0 V, I_{SENSE} = 0 V, $C_{V(CC)}$ = 0.33 μF, C_{GATE} = 1.0 nF (ESR = 10 Ω); C_{SS} = 470 pF; $C_{V(FB)}$ = 100 pF, unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
General					
I_{CC} Operating − V_{GATE} not switching	−	−	10	13	mA
I_{CC} at V_{CC} Low	V_{CC} = 6.0 V	−	500	750	μA
I_{CC} Sleep	V_{UVL} = 1.0 V	−	210	275	μA
Low V_{CC} Lockout					
V_{CC} Turn−on Threshold Voltage	−	7.2	7.7	8.3	V
V_{CC} Turn−off Threshold Voltage	−	6.8	7.3	7.8	V
V_{CC} Hysteresis	−	350	425	500	mV
UVLO					
Sleep Threshold Voltage	UVLO decreasing	1.5	1.8	2.3	V
Sleep Threshold Voltage	UVLO increasing	−	1.88	2.45	V
Sleep Hysteresis	−	35	85	150	mV
UVLO Turn−off Threshold Voltage	(Note 2)	2.3	2.45	2.6	V
UVLO Turn−on Threshold Voltage	(Note 2)	2.50	2.63	2.76	V
UVLO Hysteresis	Turn−on − Turn−off ($-40°C \le T_J \le 100°C$) (Note 2)	170	185	200	mV
UVLO Hysteresis	Turn−on − Turn−off ($100°C \le T_J \le 125°C$) (Note 2)	50	185	400	mV
UVLO Input Bias Current	−	−1.0	−	1.0	μA
UVLO Clamp	With UVLO sinking 1.0 mA	5.0	7.5	12	V
V_{CC} Clamp and BIAS Pin	**CS5124 Only. Connect an NFET as follows: BIAS = G, V_{CC} = S, V_{IN} = D.**				
V_{CC} Clamp Voltage	$36\ V \le V_{IN} \le 60\ V$, $200\ nF \le C_{SS} \le 500\ nF$, R = 500 k	7.275	7.9	8.625	V
BIAS Minimum Voltage	Measure Voltage on BIAS with: $10\ V \le V_{CC} \le 20\ V$ & $50\ \mu A \le I_{BIAS} \le 1.0\ mA$	1.6	2.8	4.0	V
BIAS Clamp	With BIAS pin sinking 1.0 mA	12	15	20	V
Difference between Regulated V_{CC} & V_{CC} Turn−on Threshold Voltage	(V_{CC} Clamp Voltage) − (V_{CC} Turn−on Threshold)	100	−	−	mV
200 kHz Oscillator	**CS5126 Only**				
Operating Frequency	−	175	200	225	kHz
Max Duty Cycle Clamp	−	78	82.5	85	%
Slope Compensation (Normal operation)	−	12	18	23	mV/μs
Slope Compensation (Synchronized operation)	(Note 2)	7.0	12	16	mV/μs
SYNC Input Threshold Voltage	−	1.0	2.0	3.0	V
SYNC Input Impedance	Measured with SYNC = 1.0 V & 10 V	50	120	230	kΩ
400 kHz Oscillator	**CS5124 Only**				
Operating Frequency	−	360	400	440	kHz
Max Duty Cycle Clamp	−	80.0	82.5	85.0	%
Slope Compensation	−	15	21	26	mV/μs

2. Not tested in production. Specification is guaranteed by design.

ELECTRICAL CHARACTERISTICS (continued) ($-40°C \le T_J \le 125°C$; $-40°C \le T_A \le 105°C$, $7.60\ V \le V_{CC} \le 20\ V$, UVLO = 3.0 V, I_{SENSE} = 0 V, $C_{V(CC)}$ = 0.33 μF, C_{GATE} = 1.0 nF (ESR = 10 Ω); C_{SS} = 470 pF; $C_{V(FB)}$ = 100 pF, unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Soft−Start					
Soft−Start Charge Current	−	7.0	10	13	μA
Soft−Start Discharge Current	−	0.5	10.0	−	mA
V_{SS} Voltage when V_{FB} Begins to Rise	V_{FB} = 300 mV	1.40	1.62	1.80	V
Peak Soft−Start Charge Voltage	−	4.7	4.9	−	V
Valley Soft−Start Discharge Voltage	−	200	275	400	mV
Current Sense	**CS5124 Only**				
First Current Sense Threshold	At max duty cycle	170	195	215	mV
Second Current Sense Threshold	−	250	275	315	mV
I_{SENSE} to GATE Prop. Delay	0 to 700 mV pulse into I_{SENSE} (after blanking time)	60	90	130	ns
Leading Edge Blanking Time	0 to 400 mV pulse into I_{SENSE}	90	130	180	ns
Internal Offset	Note 3	−	60	−	mV
Current Sense	**CS5126 Only**				
First Current Sense Threshold	At max duty cycle	300	335	360	mV
Second Current Sense Threshold	−	485	525	575	mV
I_{SENSE} to GATE Prop. Delay	0 to 800 mV pulse into I_{SENSE} (after blanking time)	60	90	130	ns
Leading Edge Blanking Time	0 to 550 mV pulse into I_{SENSE}	110	175	210	ns
Internal Offset	(Note 3)	−	125	−	mV
Voltage Feedback					
V_{FB} Pull−up Res.	−	2.9	4.3	8.1	kΩ
V_{FB} Clamp Voltage	CS5124 Only	2.63	2.90	3.15	V
V_{FB} Clamp Voltage	CS5126 Only	2.40	2.65	290	V
V_{FB} Fault Voltage Threshold	−	460	490	520	mV
Output Gate Drive					
Maximum Sleep Pull−down Voltage	V_{CC} = 6.0 V, I_{OUT} = 1.0 mA	−	1.2	2.0	V
GATE High (AC)	Series resistance < 1.0 Ω, (Note 3)	V_{CC} − 1.0	V_{CC} − 0.5	−	V
GATE Low (AC)	Series resistance < 1.0 Ω, (Note 3)	−	0.0	0.5	V
GATE High Clamp Voltage	V_{CC} = 20 V	11.0	13.5	16.0	V
Rise Time	Measure GATE rise time, 1.0 V < GATE < 9.0 V V_{CC} = 12 V	−	45	65	ns
Fall TIme	Measure GATE fall time, 9.0 V > GATE > 1.0 V V_{CC} = 12 V	−	25	55	ns
Thermal Shutdown					
Thermal Shutdown Temperature	(Note 3) GATE low	135	150	165	°C
Thermal Enable Temperature	(Note 3) GATE switching	100	125	150	°C
Thermal Hysteresis	(Note 3)	15	25	35	°C

3. Not tested in production. Specification is guaranteed by design.

PACKAGE PIN DESCRIPTION

PACKAGE PIN #		Pin	Description
CS5124	CS5126		
1	1	V_{CC}	V_{CC} Power Input Pin.
2	−	BIAS	V_{CC} Clamp Output Pin. This pin will control the gate of an N−channel MOSFET that in turn regulates Vcc. This pin is internally clamped at 15 V when the IC is in sleep mode.
−	3	SYNC	Clock Synchronization Pin. A positive edge will terminate the current PWM cycle. Ground this pin when it is not used.
3	2	UVLO	Sleep and under voltage lockout pin. A voltage greater than 1.8 V causes the chip to “wake up” however the GATE remains low. A voltage greater than 2.6 V on this pin allows the output to switch.
4	4	SS	Soft−Start Capacitor Pin. A capacitor placed between SS and GROUND is charged with 10 μA and discharged with 10 mA. The Soft−Start capacitor controls both Soft−Start time and hiccup mode frequency.
5	5	V_{FB}	Voltage Feedback Pin. The collector of an optocoupler is typically tied to this pin. This pin is pulled up internally by a 4.3 kΩ resistor to 5.0 V and is clamped internally at 2.9 V (2.65 V). If V_{FB} is pulled > 4.0 V, the oscillator is disabled and GATE will stay high. If the V_{FB} pin is pulled < 0.49 V, GATE will stay low.
6	6	I_{SENSE}	Current Sense Pin. This pin is connected to the current sense resistor on the primary side. If V_{FB} is floating, the GATE will go low if I_{SENSE} = 195 mV (335 mV). If I_{SENSE} > 275 mV (525 mV), Soft−Start will be initiated.
7	7	GATE	Gate Drive Output Pin. Capable of driving a 3.0 nF load. GATE is nominally clamped to 13.5 V.
8	8	GND	Ground Pin.

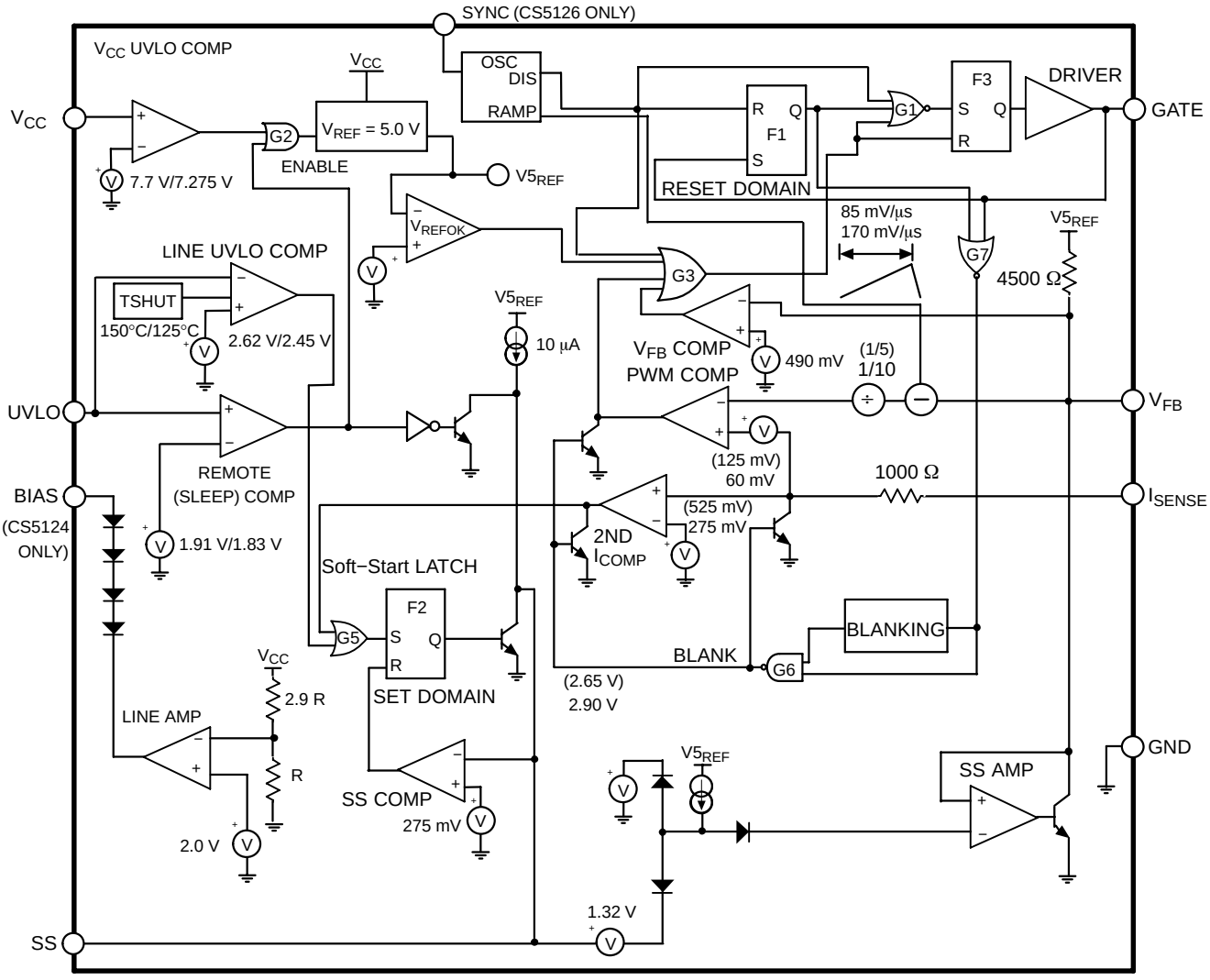


Figure 2. Block Diagram

THEORY OF OPERATION

Powering the IC

V_{CC} can be powered directly from a regulated supply and requires 500 μA of startup current. The CS5124/6 includes a line bias pin (BIAS) that can be used to control a series pass transistor for operation over a wide input voltage. The BIAS pin will control the gate voltage of an N−channel MOSFET placed between V_{IN} and V_{CC} to regulate V_{CC} at 8.0 V.

V_{CC} and UVLO Pins

The UVLO pin has three different modes; low power shutdown, Line UVLO, and normal operation. To illustrate how the UVLO pin works; assume that V_{IN}, as shown in the application schematic, is ramped up starting at 0 V with the UVLO pin open. The SS and I_{SENSE} pins also start at 0 V. While the UVLO is below 1.8 V, the IC will remain in a low current sleep mode and the BIAS pin of the CS5124 is internally clamped to a maximum of 15 V. When the voltage on the UVLO pin rises to between 1.8 V and 2.6 V the reference for the V_{CC} UVLO is enabled and V_{CC} is regulated to 8.0 V by the BIAS pin (CS5124 only), but the IC remains in a UVLO state and the output driver does not switch. When the UVLO pin exceeds 2.6 V and the V_{CC} pin exceeds 7.7 V, the GATE pin is released from a low state and can begin switching based on the comparison of the I_{SENSE} and V_{FB} pins. The Soft−Start capacitor begins charging from 0 V at 10 μA. As the capacitor charges, a buffered version of the capacitor voltage appears on the V_{FB} pin and the V_{FB} voltage begins to rise. As V_{FB} rises the duty cycle increases until the supply comes into regulation.

Soft−Start

Soft−Start is accomplished by clamping the V_{FB} pin 1.32 V below the SS pin during normal start up and during restart after a fault condition. When the CS5124/6 starts, the Soft−Start capacitor is charged from a 10 μA source from 0 V to 4.9 V. The V_{FB} pin follows the Soft−Start pin offset by −1.32 V until the supply comes into regulation or until the Soft−Start error amp is clamped at 2.9 V (2.65 V for the CS5126). During fault conditions the Soft−Start capacitor is discharged at 10 mA.

Fault Conditions

The CS5124/6 recognizes the following faults: UVLO off, Thermal Shutdown, $V_{REF(OK)}$, and Second Current Threshold. Once a fault is recognized, fault latch F2 is set and the IC immediately shuts down the output driver and discharges the Soft−Start capacitor. Soft−Start will begin only after all faults have been removed and the Soft−Start capacitor has been discharged to less than 0.275 V. Each fault will be explained in the following sections.

Under Voltage Lockout (UVLO)

The UVLO pin is tied to typically the midpoint of a resistive divider between V_{IN} and GROUND. During a start up sequence, this pin must be above 2.6 V in order for the IC to begin normal operation. If the IC is running and this pin is pulled below 1.8 V, F2 shuts down the output driver and discharges the Soft−Start capacitor in order to insure proper startup. If the UVLO pin is pulled high again before the Soft−Start capacitor discharges, the IC will complete the Soft−Start discharge and, if no other faults are present, will immediately restart the power supply. If the UVLO pin stays low, then it will enter either the low current sleep mode or the UVLO state depending on the level of the UVLO pin.

Thermal Shutdown

If the IC junction temperature exceeds approximately 150°C the thermal shutdown circuit sets F2, which shuts down the output driver and discharges the Soft−Start capacitor. If no other faults are present the IC will initiate Soft−Start when the IC junction temperature has been reduced by 25°C.

$V_{REF(OK)}$

$V_{REF(OK)}$ is an internal monitor that insures the internal regulator is running before any switching occurs. This function does not trip the fault comparator like the other fault functions. To insure that Soft−Start will occur at low line conditions the UVLO divider should be set up so that the V_{CC} UVLO comparator turns on before the LINE UVLO comparator.

Second Threshold Comparator

Since the maximum dynamic range of the I_{SENSE} signal in normal operation is 195 mV (335 mV for the CS5126), any voltage exceeding this threshold on the I_{SENSE} pin is considered a fault and the PWM cycle is terminated. The 2nd I_{COMP} compares the I_{SENSE} signal with a 275 mV (525 mV for the CS5126) threshold. If the I_{SENSE} voltage exceeds the second threshold, F2 is set, the driver turns off, and the Soft−Start capacitor discharges. After the Soft−Start capacitor has discharged to less than 0.275 V Soft−Start will begin. If the fault condition has been removed the supply will operate normally. If the fault remains the supply will operate in hiccup mode until the fault condition is removed.

V_{FB} Comparator

The V_{FB} comparator detects when the output voltage is too high. When the regulated output voltage is too high, the feedback loop will drive V_{FB} low. If V_{FB} is less than 0.49 V the output of the V_{FB} comparator will go high and shut the output driver off.

Oscillator

The internally trimmed, 400 kHz (CS5124) or 200 kHz (CS5126) provides the slope compensation ramp as well as the pulse for enabling the output driver.

PWM Comparator and Slope Compensation

The CS5124/6 provides a fixed internal slope compensation ramp that is subtracted from the feedback signal. The PWM comparator compares peak primary current to a portion of the difference of the feedback voltage and slope compensation ramp. The 170 mV/μs (85 mV/μs for the CS5126) slope compensation ramp is subtracted from the voltage feedback signal internally. The difference signal is then divided by ten (five for the CS5126) before the PWM comparator to provide high noise rejection with a low voltage across the current sense network. (The effective ramp is 21 mV/μs for the CS5124, and 18 mV/μs for the CS5126). A 60 mV (125 mV for the CS5126) nominal offset on the positive input to the PWM comparator allows for operation with the I_{SENSE} pin at, or even slightly below GND.

A 4.3 kΩ pull−up resistor internally connected to a 5.0 V nominal reference provides the bias current to for an optocoupler connection to the V_{FB} pin.

APPLICATION INFORMATION

UVLO and Thermal Shutdown Interaction

The UVLO pin and thermal shutdown circuit share the same internal comparator. During high temperature operation (T_J > 100°C) the UVLO pin will interact with the thermal shutdown circuit. This interaction increases the turn−on threshold (and hysteresis) of the UVLO circuit. If the UVLO pin shuts down the IC during high temperature operation, higher hysteresis (see hysteresis specification) might be required to enable the IC.

BIAS Pin (CS5124 Only)

The bias pin can be used to control V_{CC} as shown in the main application diagram in Figure 1. In order to provide adequate phase margin for the bias control loop, the pole created by the series pass transistor and the V_{CC} bypass capacitor should be kept above 10 kHz. The frequency of this pole can be calculated by Formula (1).

$$\text{Pole Frequency} = \frac{\text{Transconductance of pass Transistor}}{2 \times \pi \times C_{V(CC)}} \quad (1)$$

The Line BIAS pin shows a significant change in the regulated V_{CC} voltage when sinking large currents. This will show up as poor line regulation with a low value pull−up resistor. Typical regulated V_{CC} vs BIAS pin sink current is shown in Figure 3.

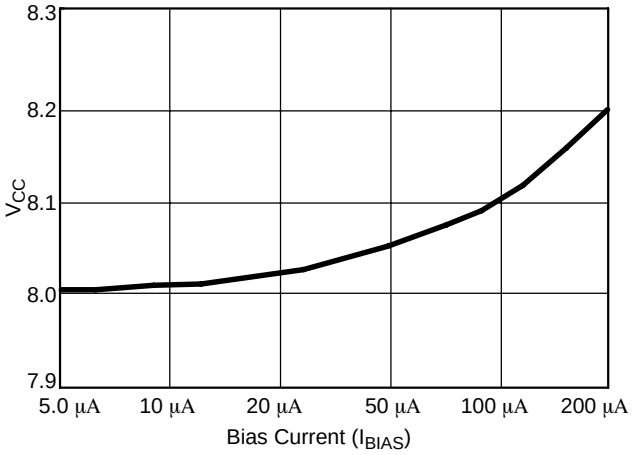


Figure 3. Regulated V_{CC} vs. BIAS Sink Current

The BIAS pin and associated components form a high impedance node. Care should be taken during PCB layout to avoid connections that could couple noise into this node. To ensure adequate design margin between the regulated V_{CC} and the Low V_{CC} Lockout voltage, a guaranteed minimum differential between the two values is specified (see electrical characteristcs).

Clock Synchronization Pin (CS5126 Only)

The CS5126 can be synchronized to signals ranging from 30% slower to several times faster than the internal oscillator frequency. If the part is synchronized to a fast signal, maximum duty cycle will be reduced as the frequency increases as shown in Figure 4.

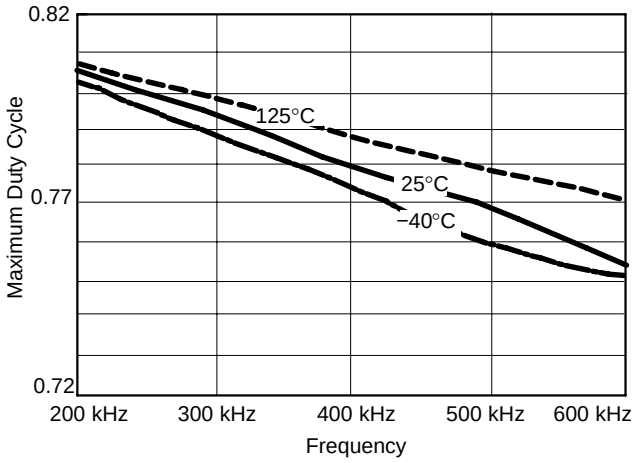


Figure 4. CS5126 Maximum Duty Cycle vs. Frequency (Synchronized Operation)

If the converter is initially free running and a sync signal is applied, the current oscillator cycle will terminate and the oscillator will lock on to the sync signal. The SYNC pin works with a positive edge triggered signal. When the sync signal transitions high the current PWM cycle terminates and a new cycle begins as shown in Figure 5. The typical phase lag between the rising edge of the SYNC signal and the rising edge of the Gate is shown in Figure 6. When this pin is held high or low the internal clock determines the oscillator frequency.

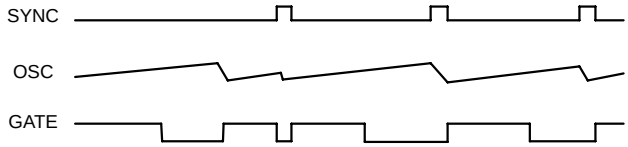


Figure 5. Synchronized Operation

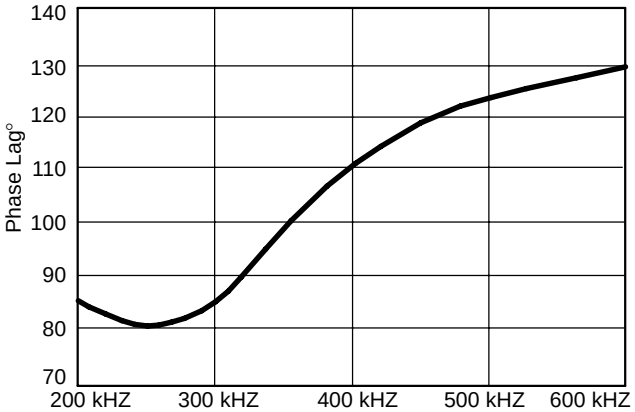


Figure 6. Typical Phase Lag between SYNC and GATE on

Gate Drive

Rail to rail gate driver operation can be obtained (up to 13.5 V) over a range of MOSFET input capacitance if the gate resistor value is kept low. Figure 5 shows the high gate drive level vs. the series gate resistance with V_{CC} = 8.0 V driving an IRF220.

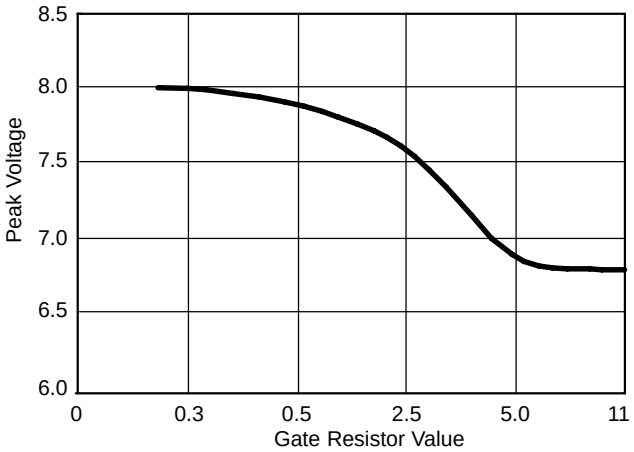


Figure 7. Gate Drive vs. Gate Resistor Driving an IRF220 (V_{CC} = 8.0 V)

A large negative dv/dt on the power MOSFET drain will couple current into the gate driver through the gate to drain capacitance. If this current is kept within absolute maximum ratings for the GATE pin it will not damage the IC. However if a high negative dv/dt coincides with the start of a PWM duty cycle, there will be small variations in oscillator frequency due to current in the controller substrate. If required, this can be avoided by choosing the transformer ratio and reset circuit so that a high dv/dt does not coincide with the start of a PWM cycle, or by clamping the negative voltage on the GATE pin with a Schottky diode

First Current Sense Threshold

During normal operation the peak primary current is controlled by the level of the V_{FB} pin (as determined by the control loop) and the current sense network. Once the signal on the I_{SENSE} pin exceeds the level determined by V_{FB} pin the PWM cycle terminates. During high output currents the V_{FB} pin will rise until it reaches the V_{FB} clamp. The first current sense threshold determines the maximum signal allowed on the I_{SENSE} pin before the PWM cycle is terminated. Under this condition the maximum peak current is determined by the V_{FB} Clamp, the slope compensation ramp, the PWM comparator offset voltage and the PWM on time. The nominal first current threshold varies with on time and can be calculated from Formulas (2) and (3) below.

CS5124

$$\text{1st Threshold} = \frac{2.9\ \text{V} - 170\ \text{mV}/\mu\text{s} \times T_{ON}}{10} - 60\ \text{mV} \qquad (2)$$

CS5126

$$\text{1st Threshold} = \frac{2.65\ \text{V} - 85\ \text{mV}/\mu\text{s} \times T_{ON}}{5.0} - 125\ \text{mV} \qquad (3)$$

When the output current is high enough for the I_{SENSE} pin to exceed the first threshold, the PWM cycle terminates early and the converter begins to function more like a current source. The current sense network must be chosen so that the peak current during normal operation does not exceed the first current sense threshold.

Second Current Sense Threshold

The second threshold is intended to protect the converter from overheating by switching to a low duty cycle mode when there are abnormally high fast rise currents in the converter. If the second current sense threshold is tripped, the converter will shut off and restart in Soft−Start mode until the high current condition is removed. The dead time after a second threshold overcurrent condition will primarily be determined by the time required to charge the Soft−Start cap from 0.275 V nominal to 1.32 V.

The second threshold will only be reached when a high dv/dt is present at the current sense pin. The signal must be fast enough to reach the second threshold before the first threshold turns off the driver. This will normally happen if the forward inductor saturates or when there is a shorted load.

Excessive filtering of the current sense signal, a low value current sense resistor, or even an inductor that does not saturate during heavy output currents can prevent the second threshold from being reached. In this case the first current sense threshold will trip during each cycle of high output current conditions. The first threshold will limit output current but some components, especially the output rectifier, can overheat due to higher than normal average output current.

Slope Compensation

Current mode converters operating at duty cycles in excess of 50% require an artificial ramp to be added to the current waveform or subtracted from the feedback waveform. For the current loop to be stable the artificial ramp must be equivalent to at least 50% of the inductor current down slope and is typically chosen between 75% to 100% of the inductor down current down slope.

To choose an inductor value such that the internal slope compensation ramp will be equal to a certain fraction of the inductor down current slope use the Formula (4).

$$\frac{1}{\text{Internal Ramp}} \times (V_{OUT} + V_{RECTIFIER}) \times \frac{N_{SECONDARY}}{N_{PRIMARY}} \times R_{SENSE} \times \text{Slope Value Factor} = \text{Inductor Value(H)} \qquad (4)$$

Calculating the nominal inductor value for an artificial ramp equivalent to 100% of the current inductor down slope at CS5126 nominal conditions, a 5.0 V output, a 200 mΩ current sense resistor and a 4:1 transformer ratio yields

$$\frac{1}{20\ \text{mV}/\mu\text{s}} \times (5.0\ \text{V} + 0.3\ \text{V}) \times \frac{1}{4} \times 0.2\ \Omega \times 1.0 = 13.2\ \mu\text{H} \qquad (5)$$

To check that the slope compensation ramp will be greater than 50% of the inductor down under all conditions, substitute the minimum internal slope compensation value and use 0.5 for the slope compensation value. Then check that the actual inductor value will always be greater than the inductor value calculated.

During synchronized operation of the CS5126 the slope compensation ramp is reduced by 33%. If the CS5126 will be used in synchronized operation, the inductor value should be recalculated to work with the slope compensation ramp reduced to 67% of the normal value.

Powering the CS5124/6 from a Transformer Winding

There are numerous ways to power the CS5124/6 from a transformer winding to enable the converter to be operated at high efficiency over a wide input range. Two ways are shown in the application circuits.

The CS5124 application circuit in Figure 1 is a flyback converter that uses a second flyback winding to power V_{CC}. R4 improves V_{CC} regulation with load changes by snubbing the turn off spike. Once the turn off spike has subsided the voltage of this winding is voltage proportional to the voltage on the main flyback winding. This voltage is regulated because the main winding is clamped by the regulated output voltage.

In the CS5126 application circuit in Figure 8 an extra winding is added to the forward inductor to power V_{CC}. This winding is phased to conduct during the off time of the forward converter and performs the same function as the flyback winding above.

A flyback winding from a forward transformer can also be used to power V_{CC}. Ideally the transformer volt−second product of a forward converter would be constant over the range of line voltages and load currents; and the transformer inductance could be chosen to store the required level of energy during each cycle to power V_{CC}. Even though the flyback energy is not directly regulated it would remain constant. Unfortunately in a real converter there are many nonideal effects that degrade regulation. Transformer inductance varies, converter frequency varies, energy stored in primary leakage inductance varies with output current, stray transformer capacitances and various parasitics all effect the level of energy available for V_{CC}. If too little energy is provided to V_{CC}, the bootstrapping circuit must provide power and efficiency will be reduced. If too much energy is provided V_{CC} rises and may damage the controller. If this approach is taken the circuit must be carefully designed and component values must be controlled for good regulation.

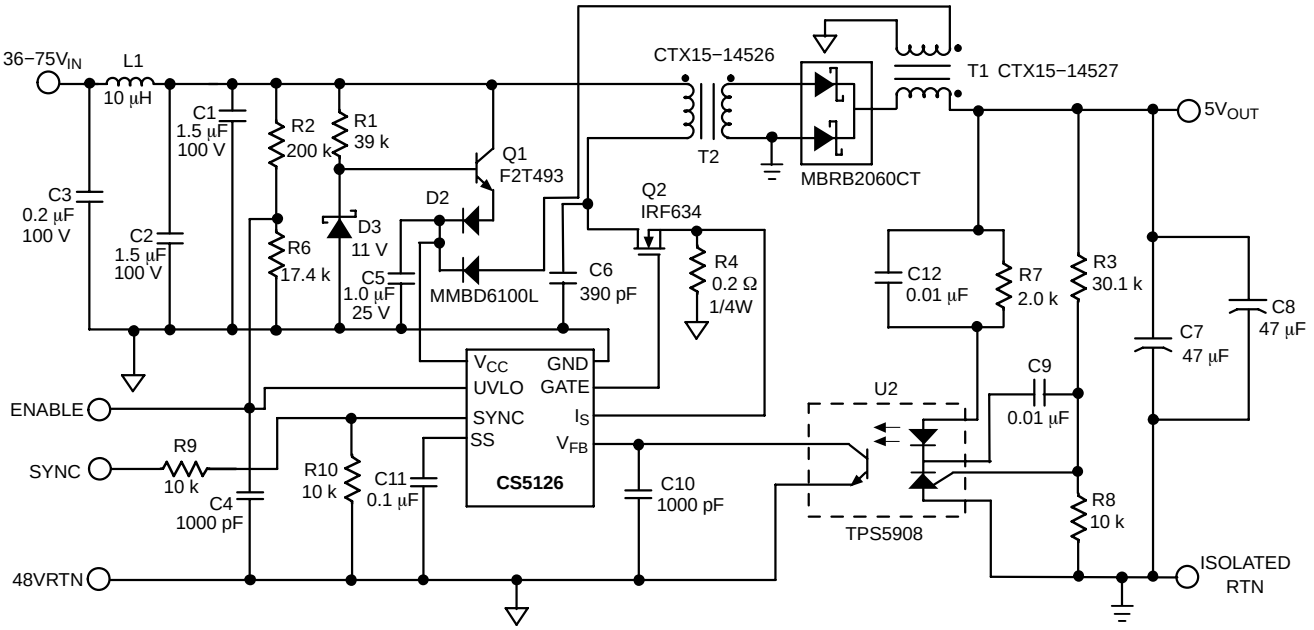
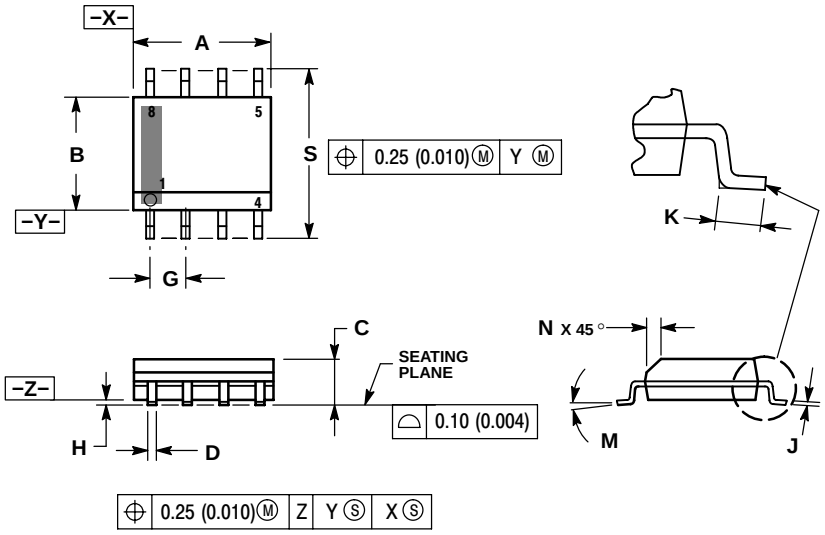


Figure 8. Additional Application Diagram, 48 V to 5.0 V, 5.0 A Forward Converter using the CS5126

PACKAGE DIMENSIONS

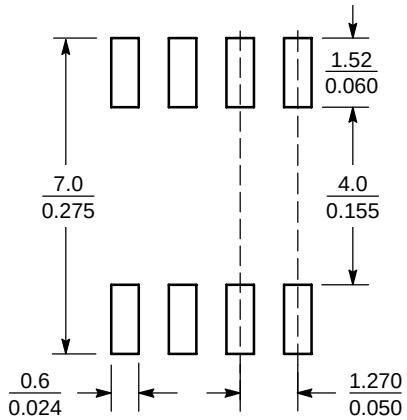
SOIC−8
D SUFFIX
CASE 751−07
ISSUE AG



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE THERMAL DATA

Parameter		SOIC−8	Unit
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$R_{\theta JA}$	Typical	165	°C/W

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